AN-1032 An Introduction to FPD-Link

ABSTRACT

The FPD-Link chipset architecture in conjunction with the LVDS technology provides the high bandwidth interface necessary for leading edge display technology. The conversion from parallel TTL to serial LVDS allows for a narrow interface between graphics controller and panel. A narrower interface means lower cable cost and simplifies the physical connection through a notebook hinge. The high speed of the LVDS technology supports the high data transfer rates required. EMI problems typically associated with such high speed transmissions are addressed by the low signal swing and differential nature of LVDS. LVDS, with its high speed capabilities, will allow future products in the FPD-Link chipset to support the industry's ever increasing needs for bandwidth. Texas Instrument's FPD-Link provides the solution for the latest in display technology.

Contents

List of Figures

TRI-STATE is a registered trademark of Texas Instruments.

1 The FPD-Link Chipset

The FPD-Link (Flat Panel Display Link) chipset is a family of interface devices specifically configured to support data transmission from graphics controller to LCD panels. The technology employed, LVDS (Low Voltage Differential Signaling), is ideal for high speed, low power data transfer. This enables the implementation of high end displays such as SVGA (800 x 600) and XGA (1024 x 768).

The predominant issues limiting performance in these high end displays are speed, power, and EMI considerations. The user is also concerned with the physical interface to the display; the fewer wires the better. The FPD-Link chipset addresses these issues with LVDS technology and muxing TTL signals to higher speed LVDS signals which allows a substantially narrower interface between host and display. In a typical application (see Figure 1), TTL-level RGB and control data from the graphic controller arrives at the inputs of the FPD-Link transmitter. The parallel TTL data is muxed and converted to LVDS. The outputs of the FPD-Link transmitter drive the LVDS data on the cable which connects the motherboard to the display. The LVDS data traverses the cable to the FPD-Link receiver at the display. The received data is then demuxed, converted back to TTL levels and sent to the inputs of the timing controller. This muxing of parallel TTL signals allows the data to travel at faster speeds across a narrow interface, addressing needs associated with high bandwidth communication.

The FPD-Link chipset consists of transmitters (TTL to LVDS) and receivers (LVDS to TTL) designed to support 18-bit and 24-bit color displays. Devices are available with falling edge, rising edge or programmable data strobe for a convenient interface to a variety of graphics and LCD panel controllers. The FPD-Link product family includes 5V and 3.3V chipsets that support a frequency range of 20 MHz to 65 MHz. See Figure 2.
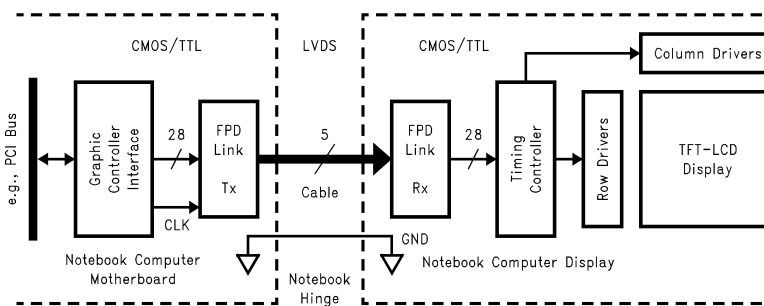

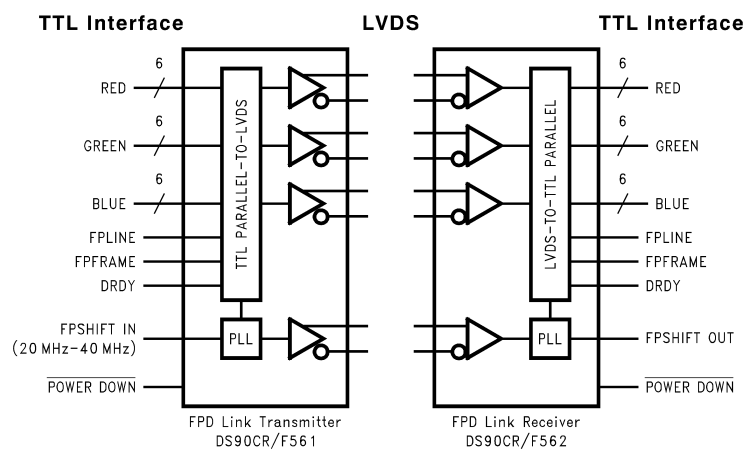**Figure 1. Typical FPD-Link Application (24-Bit Color)**

Figure 2. FPD-Link Chipset for 18-Bit Color

2   LVDS-The Technology Of Choice

LVDS is a differential signaling technology designed to support applications requiring high speed data transfer, common mode noise rejection, and low power consumption. The low signal swing (345 mV) and differential nature of the signals reduces noise impact (i.e., crosstalk) and allows high operating frequencies. The constant current source is designed for low power consumption: a single LVDS driver has a static I_{CC} of 4 mA and dynamic I_{CC} of 22 mA. These attributes contribute to the low EMI of LVDS.

3   Designing With FPD-link

The FPD-Link chipset provides the support needed for high speed display interfaces such as SVGA(800 x 600) and XGA(1024 x 768). Care should be taken when designing with these devices to fully realize the benefits of the technology.

Board Layout. To obtain the maximum benefit from the noise and EMI reductions of LVDS, attention should be paid to the layout of differential lines. Lines of a differential pair should always be adjacent to eliminate noise interference from other signals and take full advantage of the noise canceling of the differential signals. The board designer must also maintain equal length on the signal traces for a given pair. As with any high speed design, the impedance discontinuities should be limited (reduce number of vias, no 90° angles on traces). Any discontinuities which do occur on one signal line should be mirrored in the other line of the differential pair. These considerations limit reflections and crosstalk which would adversely effect high frequency performance and EMI.

24-Bit to 18-Bit Interface. It may be necessary to interface a 24-bit transmitter to an 18-bit receiver (or vice-versa). In this case, the least significant color bits of the 24-bit transmitter are mapped to the fourth LVDS channel. Three LVDS data channels are connected to the 18-bit receiver; the remaining fourth LVDS data channel is left open.

Termination. Use of current mode drivers requires a terminating resistor across the receiver inputs. The FPD-Link chipset uses a single 100Ω resistor between the positive and negative lines of each receiver differential pair (see Figure 3). No additional pull-up or pull-down resistors are necessary as with some other differential technologies (PECL). Surface mount resistors are recommended to avoid the additional inductance that accompanies leaded resistors. These resistors should be placed as close as possible to the receiver input pins to reduce stubs and effectively terminate the differential lines.
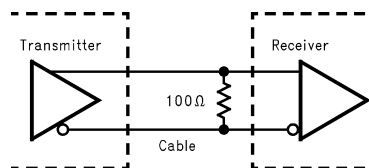

Figure 3. FPD-Link Termination

Decoupling Capacitors. Bypassing capacitors are needed to reduce the impact of switching noise which could limit performance. Decoupling capacitors (surface mount) between each V_{CC} and ground pin are recommended. Refer to Figure 4 for an example of connections and capacitor values.
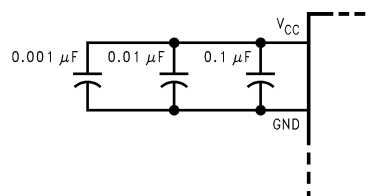

Figure 4. Decoupling Configuration

Cables. A cable interface between the transmitter and receiver needs to support the differential LVDS pairs (2 wires/pair). The 8-bit chipsets require 10 signal wires; the 6-bit chipsets require 8 signal wires. This is a significant reduction in cable width as compared to the straight TTL interface which needs 28 or 21 signal wires. Shielded cables will reduce noise emissions that contribute to EMI. In addition, ground lines between each differential pair will provide further noise shielding. The grounding provides a barrier to noise coupling between adjacent pairs, thus reducing additive effects of the electrical fields. In addition to the noise shielding, the low impedance ground connection between the transmitter and receiver provides a common mode return path. A minimum of two ground conductors is recommended to provide this low impedance path.

An ideal cable/connector interface would have a constant 100Ω differential impedance throughout the path. It is recommended that cable skew remain below 250 ps (at 65MHz) to help maintain a sufficient data sampling window. Edge rate attenuation should also be limited to avoid signal degradation at high frequencies. Both skew and edge rate attenuation are a function of cable length. As the distance between host and display increases, a higher quality cable is needed to preserve signal integrity.

Though the interconnect between host and LCD is typically short, the FPD-Link transmitters can drive cables over 5 meters long. This makes the FPD-Link useful for remote display applications.

4   TTL To LVDS Translation

The FPD-Link transmitter translates 21 or 28 bit wide TTL data into LVDS data 3 or 4 bits wide and 7 bits deep. An additional pair of LVDS signals is used to transmit the clock. All 21/28 parallel TTL bits are transferred with a single data strobe. A single strobe also transmits all bits at the LVDS port. The clock to data relationship at the LVDS interface is shown in Figure 5. The clock at the LVDS ports is transmitted at the TTL clock input frequency (i.e., 65 MHz); the data is transmitted at 3.5 times the clock frequency (227 MHz).

The TTL data bits are mapped into the 3 or 4 LVDS signal lines. Figure 6 and Figure 7 show the relationship of parallel TTL data bits to the LVDS link.
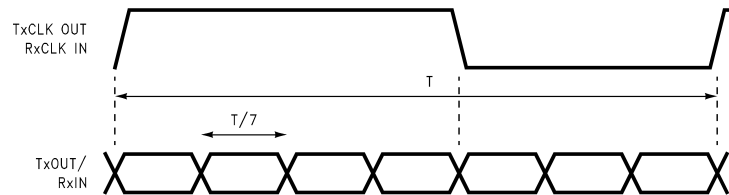

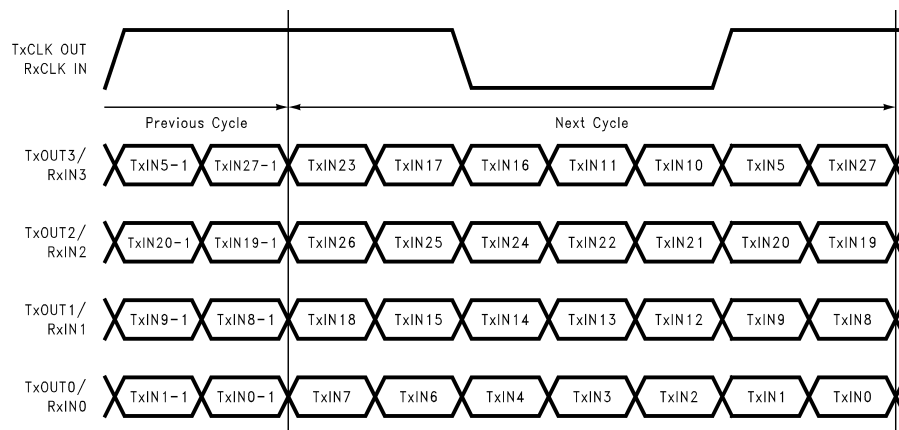**Figure 5. Seven Bits of LVDS in One Clock Cycle**

Figure 6. 28 Parallel TTL Data Inputs Mapped to LVDS Outputs (DS90CR581)
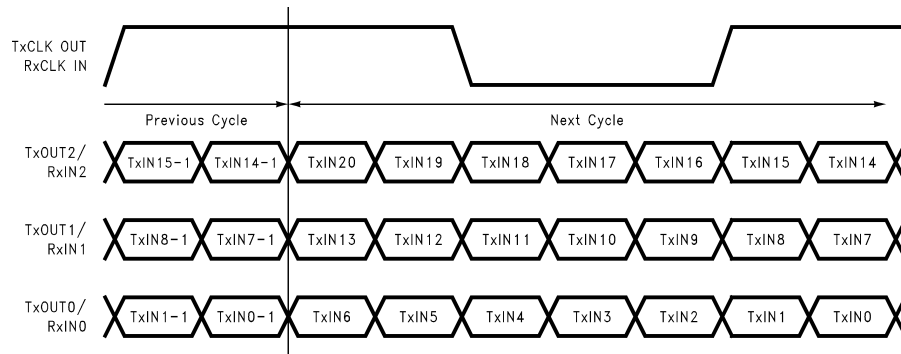
Figure 7. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs (DS90CR561)

5 Power Sequencing

Outputs of the FPD-Link transmitter remain in TRI-STATE® until the power supply reaches 3V. The receiver outputs are low when powerdown is asserted. Clock and data outputs will begin to toggle 10 ms after V_{CC} has reached 3V and the Powerdown pin is above 2V.

When powering down the device, the Powerdown pin may be asserted. This will TRI-STATE the transmitter outputs to prevent excess current flow (55 µA maximum). This input is typically driven by power supply control logic.

The FPD-Link chipset is designed to protect itself from accidental loss of power to either the transmitter or receiver. If power to the transmit board is lost, the receiver clocks (input and output) stop. The data outputs (RxOUT) retain the states they were in when the clocks stopped. When the receiver board loses power, the receiver inputs are shorted to V_{CC} through a diode. Current is limited (5 mA per input) by the fixed current mode drivers, thus avoiding the potential for latchup when powering the device. (Note: latchup immunity is > 300 mA) In addition, an external circuit can be used such that when the receiver board powers down, the transmit Powerdown pin is pulled low to TRI-STATE the transmitter outputs so short circuit current does not flow.

6 Data Strobes

The FPD-Link transmitters are available with a falling edge or selectable data strobe. A rising or falling edge strobe device should be selected based on the characteristics of the VGA controller being used. The receiver is available with a falling edge strobe to match flat panel timing controller requirements. The strobe edge only effects the TTL inputs of the transmitter or outputs of the receiver. The LVDS interface is not impacted, therefore, rising and falling edge transmitters and receivers are fully interoperable.

7 Clock Jitter Considerations

The FPD-Link devices employ a PLL to generate and recover the clock transmitted across the LVDS interface. These high speed signals require an accurate, low noise clock signal. The width of the LVDS data bits is one seventh the clock period. For example, a 40 MHz clock has a period of 25 ns; the width of a data bit is 3.6 ns. Differential signal skew, interconnect skew, data and clock jitter all reduce the available window for sampling data. It is recommended to keep each component as small as possible to support the maximum operating frequency. The initial clock source should provide a clean signal to the Tx clock input. Individual bypassing of each V_{CC} to ground will minimize the noise passed on to the PLL, thus creating a low jitter LVDS clock. These measures provide more margin for channel-to-channel skew and interconnect skew as a part of the overall jitter/skew budget.

8 EMI Benefits

One of the benefits to using the FPD-Link chips with their LVDS signaling is the relatively low EMI. LVDS has demonstrated lower spectral content (EMI) than competing technologies such as RS-422, PECL, and CMOS (often used in display interface applications). Testing was performed using DCM (direct contact method) with a 32 MHz continuous wave. Low EMI translates to less noise on a cable in a box-to-box transmission environment. The cable shielding requirements are less, thus the cost of interconnect is reduced.

9 Conclusion

The FPD-Link chipset architecture in conjunction with the LVDS technology provides the high bandwidth interface necessary for leading edge display technology. The conversion from parallel TTL to serial LVDS allows for a narrow interface between graphics controller and panel. A narrower interface means lower cable cost and simplifies the physical connection through a notebook hinge. The high speed of the LVDS technology supports the high data transfer rates required. EMI problems typically associated with such high speed transmissions are addressed by the low signal swing and differential nature of LVDS. LVDS, with its high speed capabilities, will allow future products in the FPD-Link chipset to support the industry's ever increasing needs for bandwidth. TI's FPD-Link provides the solution for the latest in display technology.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		Applications	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		